UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/910,447	07/19/2001	Toshihiko Higuchi	81754.0064	2754

26021 7590 05/28/2004

HOGAN & HARTSON L.L.P.
500 S. GRAND AVENUE
SUITE 1900
LOS ANGELES, CA 90071-2611

EXAMINER	
LE, THAO X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/910,447	HIGUCHI, TOSHIHIKO	
	Examiner	Art Unit	
	Thao X Le	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,7,9,11,21-24,28,29,31,32,34-36,38-40 and 42-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7,9,11,21-24,28,29,31,32,34-36,38-40 and 42-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Acknowledgement

1. Applicant's cancellation of claims 5-6, 8, 10, 12-20, 25-27, 30, 33, 37, 41 in the amendment file on 02 Feb. 2004 is acknowledged.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1 and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5747356 to Lee at al.

Regarding claims 1, Lee discloses a semiconductor device in fig. 3 comprising: a semiconductor substrate 1, column 2 line 29, having a indented section (where oxide 14, fig. 4b, is removed), fig. 4D, a gate dielectric 15, column 3 line 60, disposed on the indented section fig. 4d, a gate electrode 16, column 3 line 65, disposed on the gate dielectric layer 15, wherein a portion of the gate electrode 16 is embedded in the semiconductor substrate 1 and another portion of the gate electrode is above the semiconductor substrate, first and second impurity diffusion layers 18 and 17, column 4 lines 12, disposed in the semiconductor substrate 1 and opposed to each other with the gate electrode being interposed between them, a third impurity diffusion layer 19, column 3 line 18, disposed in a portion immediately below the gate electrode

in the semiconductor substrate 1, a sidewall dielectric layer 13', column 3 line 21, disposed on the side surface section of the gate electrode 16, wherein the gate electrode 16 has a width that gradually increases from a bottom thereof up to an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers 17/18 are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, and wherein the majority of the gate electrode 16 and a majority of the sidewall dielectric layer 13' are above the semiconductor substrate 1 and first and second impurity diffusion layers 17 and 18.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-2, 4, 7, 22-24, 28, 31-32, 34, 35-36, 38-39, 40, 42-60, and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6201278 to Gardner et al. in view of US 5747356 to Lee et al.

Regarding claims 1, 32, 34, 38, and 63, Gardner discloses a semiconductor device in fig. 1A-5K comprising: a semiconductor substrate 502 (or 102), column 12 line 62, having a indented section 514, fig. 5D, a gate dielectric 524 (or 124), column 13 line 57, disposed on the indented section, fig. 5H, a gate electrode 530 (or 130), column 13 line 66, disposed on the gate dielectric layer 524, wherein a portion of the gate electrode 530 is embedded in the

semiconductor substrate 502 and another portion of the gate electrode is above the semiconductor substrate (the semiconductor substrate comprises a top surface 504 and oxide layers 526A/526B, the gate electrode 530 shows above the top surface 504) first and second impurity diffusion layers 508A and 508B, column 13 line 49, disposed in the semiconductor substrate and opposed to each other with the gate electrode being interposed between them, a third impurity diffusion layer P-, fig. 5G, disposed in a portion immediately below the gate electrode in the semiconductor substrate, a sidewall dielectric layer 522A and 522B, column 13 line 38, disposed on the side surface section of the gate electrode 530, wherein the gate electrode has a width that gradually increases from a bottom thereof up to an upper surface thereof, and wherein surfaces of the first and second impurity diffusion layers are located at a position higher than an interface between the semiconductor substrate and the gate dielectric layer, fig. 5K or 1J.

But Gardner does not expressly disclose the device wherein the majority of the gate electrode and a majority of the sidewall dielectric layer are above the semiconductor substrate and first and second impurity diffusion layers.

However, Lee reference discloses the device wherein the majority of the gate electrode 16 and a majority of the sidewall dielectric layer 13' are above the semiconductor substrate 17 and first and second impurity diffusion layers 18/17, fig. 3. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the gate and sidewall teaching of Lee with Gardner's device, because it would have created a device having short length gate and shallow source and drain for memory chip or for device requiring rapid operating frequencies as taught by Lee, column 1 line 45-53.

Regarding to claim 2, Gardner discloses the semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric between about 0.20 μm, column 3 line 10.

Regarding to claim 3, Gardner discloses a semiconductor device wherein the groove section 514, column 13 line 11, is disposed at a specified location in the semiconductor substrate, and the gate electrode 530 is disposed on a bottom surface of the groove section through the gate dielectric layer 524, fig 5a-5K.

Regarding to claims 4, 7, Gardner discloses a semiconductor device wherein the gate electrode 530 may be disposed by depositing the conductive material or semiconductor material, at least one alloy that includes at least two constituents selected from polycrystalline silicon, tungsten, tantalum, copper and gold, column 13 line 66 and column 14 line 61, wherein the first and second impurity diffusion layers include an extension 552A/552B, fig. 5K.

Regarding claims 22-24, 28, and 31, Gardner discloses the semiconductor device wherein a distance between the surface of the first and second impurity diffusion layers and the interface between the semiconductor substrate and the gate dielectric between about 0.20 μm, column 3 line 10 (channel length), wherein the groove section 514, column 13 line 11, is disposed at a specified location in the semiconductor substrate, and the gate electrode 530 is disposed on a bottom surface of the groove section through the gate dielectric layer 524, fig 5a-5K, wherein the gate electrode 530 is disposed from at least one alloy that includes at least two constituents selected from polycrystalline silicon, tungsten, tantalum, copper and gold, column 13 line 66 and column 14 line 61, wherein the a third impurity diffusion layer P-, fig. 5J, immediately below the gate electrode in the semiconductor substrate, and wherein the first and second impurity

diffusion include an extension region N', fig. 1J or 5K wherein the sidewall dielectric layer 522A/522B is formed from a material including silicon oxide, column 13 line 38, wherein the sidewall dielectric layer 522A/522B or 122A/122B has an outer surface that is generally vertical with respect to the surface of the semiconductor substrate, and film thickness that gradually reduces from a bottom thereof up to an upper surface thereof, fig. 1J and 5K.

Regarding claims 35, 39, 40, 42-43, Gardner discloses the semiconductor device wherein the third impurity diffusion layer P- is completely disposed between the first and second impurity diffusion layers, fig. 1J or 5K, wherein the extension regions 132A/132B are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions, fig. 1J.

Regarding claim 36, Gardner discloses the extension regions 132A/132B are below the sidewall dielectric layer, and wherein an area below the gate dielectric layer is free of the extension regions, fig. 1J.

Regarding claims 44-48, 50, 56-60 Gardner discloses the gate electrode 130 has a width the continuously increase from the bottom thereof up to an upper surface thereof, wherein the semiconductor substrate has a first surface and the indented section 114, fig. 1D, has a second surface below the first surface, and wherein the entire gate dielectric layer 124 is disposed on the second surface, wherein the sidewall 122A/122B dielectric layer and the gate dielectric layer 124 are disposed in contact with the indented section.47, wherein the sidewall dielectric layer has an outer surface that is substantially vertical with respect to the first surface of the semiconductor substrate, wherein the sidewall dielectric layer 122A/122B surrounds the gate dielectric layer

124, and wherein at least a portion of the gate dielectric layer is above at least a portion of the sidewall dielectric layer.

Regarding claims 49-55, Gardner discloses the semiconductor device wherein at least a portion of the gate dielectric layer is above at least a portion of the sidewall dielectric layers and wherein the sidewall dielectric layer 122A is formed below the second metal silicide layer, wherein a the gate electrode is above the semiconductor substrate, the first impurities diffusion layer, and the second impurity diffusion layer 51, wherein the gate electrode has a width that continuously increase from a bottom thereof up to an upper surface thereof, wherein the semiconductor substrate has a first surface (top) and the indented section has a second surface below the first surface, and wherein the entire gate dielectric layer 124 is disposed on the second surface, wherein the sidewall dielectric layer 122A and the gate dielectric layer 124 are disposed in contact with the indented section, wherein the sidewall dielectric layer 122A surrounds the gate dielectric layer 124, wherein at a portion of the gate dielectric layer 124 is above at least a portion of the sidewall dielectric layer 122A.

6. Claims 9, 11, 21, 29, and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6201278 to Gardner et al. and US 5747356 to Lee et al. and further in view of US 6214679 to Murthy et al.

Regarding claims 9, 29, 61, Gardner does not expressly disclose the semiconductor device wherein the first metal silicide layer is disposed on the first and second impurity diffusion layers, and the gate electrode includes a second metal silicide layer on an upper surface thereof.

But Murthy reference discloses the semiconductor device wherein the metal silicide layer 236 is formed on the first and second impurity diffusion layers 218, and the

gate electrode 206 includes a metal silicide layer 236, fig. 12, on an upper surface thereof. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use silicide layer teaching of Murthy with Gardner, because it would have reduced the resistance of polysilicon as taught by Murthy, column 1 lines 47-48.

Regarding claims 11, 62, Gardner does not expressly disclose the semiconductor device wherein the surface of the first and second impurity diffusion layers are formed at a position higher than a surface of the STI.

But Murthy reference discloses the semiconductor device in fig. 12 wherein the surface of the first and second impurity diffusion layers 218 are formed at a position higher than a surface of the STI. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the elevated source and drain teaching of Murthy with Gardner's device, because it would have increased the conductivity and good punch through characteristics obtained as taught by Murthy, column 5 lines 62-67.

Regarding claim 21, as discussed in the above claim 1 Gardner discloses all the limitations of claim 21, except the surface of the first and second impurity diffusion layers are disposed at a position higher than a surface of the STI.

But Murthy reference discloses the semiconductor device in fig. 12 wherein the surface of the first and second impurity diffusion layers 218 are formed at a position higher than a surface of the STI. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the elevated source and drain teaching of

Murthy with Gardner's device, because it would have increased the conductivity and good punch through characteristics obtained as taught by Murthy, column 5 line 62-67.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is (571) 272-1708. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on (571) 272 -1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thao X. Le
14 May 2004

LONG PHAM
PRIMARY EXAMINE